

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,995,412 B2
APPLICATION NO. : 10/063331
DATED : February 7, 2006
INVENTOR(S) : Fried et al.

Page 1 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page, showing an illustrative figure, should be deleted and substitute therefor the attached title page.

In Drawings

Delete drawing sheet 7 of 8 and substitute therefor the attached sheet 7 of 8 containing figures 7A and 7B.

Column 2

Line 10, delete "length also" and insert -- length (also --

Column 10

Line 7, insert -- . -- after T_{cl}

Lines 9 and Line 20, delete "7a - 7h" and insert -- 7a - 7b --

Line 12, delete "in die claims" and insert -- in the claims --

Line 13, delete "arc" and insert -- are --

Column 12

Line 34, delete "greeter" and insert -- greater --

Line 60, delete "sonic" and insert -- same --

Column 13

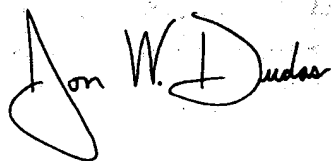
Line 34, delete "suicide" and insert -- silicide --

Column 14

Line 56, delete "or" and insert -- of --

Signed and Sealed this

Twenty-fourth Day of October, 2006

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is written in a cursive style with a large, stylized "J" and "D".

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Fried et al.

(10) Patent No.: **US 6,995,412 B2**
 (45) Date of Patent: **Feb. 7, 2006**

(54) **INTEGRATED CIRCUIT WITH CAPACITORS HAVING A FIN STRUCTURE**

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Edward J. Nowak, Essex Junction, VT (US)

(73) Assignee: **International Business Machines Corporation, Armonk, NY (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 30 days.

(21) Appl. No.: **10/063,331**

(22) Filed: **Apr. 12, 2002**

(65) **Prior Publication Data**

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(51) Int. Cl.
H01L 27/108 (2006.01)
H01L 29/76 (2006.01)
H01L 29/94 (2006.01)
H01L 31/119 (2006.01)

(52) U.S. Cl. **257/296; 257/303; 257/306**

(58) **Field of Classification Search** **257/296,**
257/300, 301, 303, 306, 68, 71, 313, 516,
257/532, 528, 535

See application file for complete search history.

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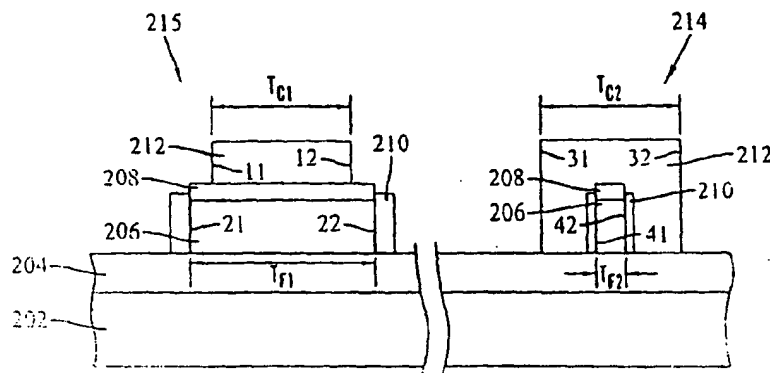
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(57) **ABSTRACT**

Device designs and methods are described for incorporating capacitors commonly used in planar CMOS technology into a FinFET based technology. A capacitor includes at least one single-crystal Fin structure having a top surface and a first side surface opposite a second side surface. Adjacent the top surface of the at least one Fin structure is at least one insulator structure. Adjacent the at least one insulator structure and over a portion of the at least one Fin structure is at least one conductor structure. Decoupling capacitors may be formed at the circuit device level using simple design changes within the same integration method, thereby allowing any number, combination, and/or type of decoupling capacitors to be fabricated easily along with other devices on the same substrate to provide effective decoupling capacitance in an area-efficient manner with superior high-frequency response.

13 Claims, 8 Drawing Sheets



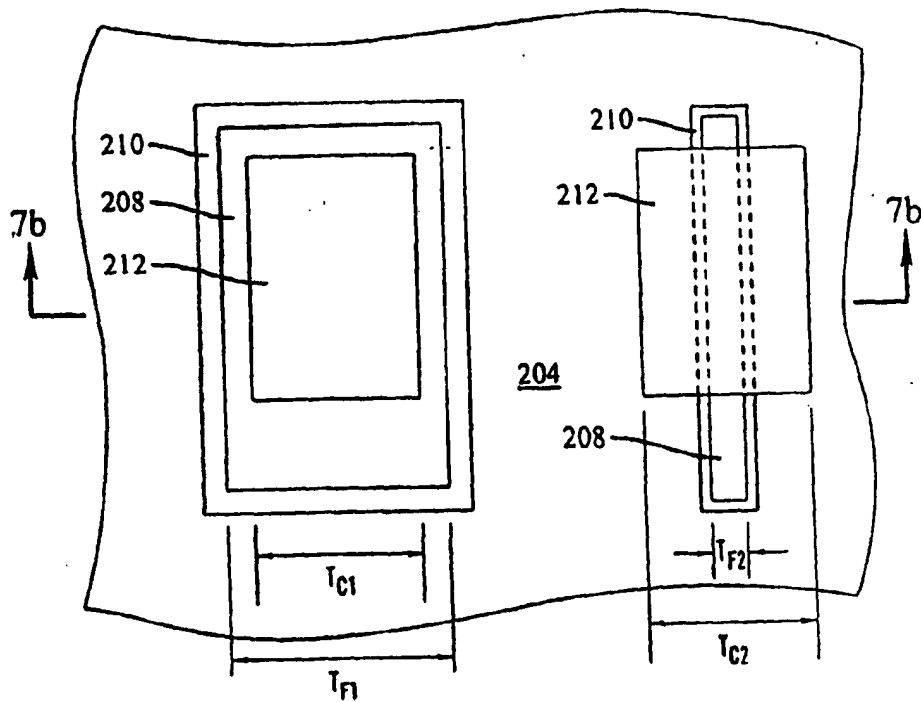


FIG. 7a

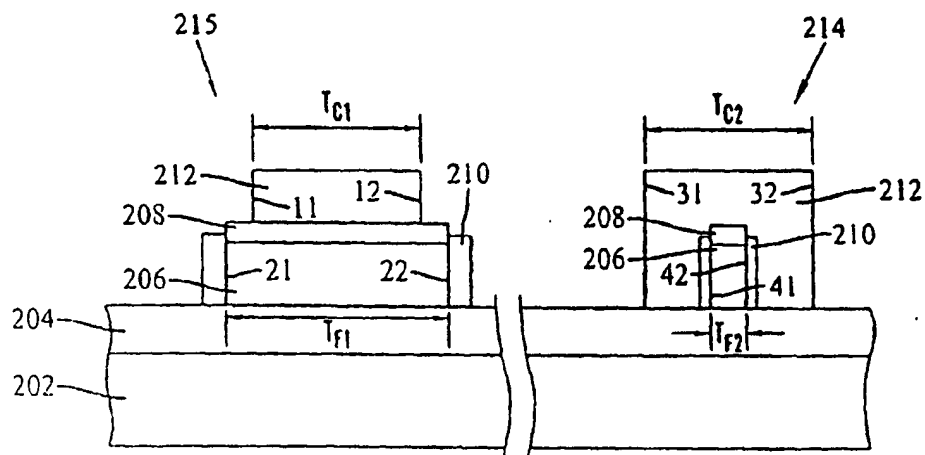


FIG. 7b